On-line resolution switching of the resolver to digital converter within a positioning servo drive comprising simulated encoder

Mario Salano, Franco Talpone and Franco Tarantini, Vickers Electrics,
via Avosso 94, 16015 Casella (GE), Italy
Peric S. Ljiljana and Slobodan N. Vukosavic, Electrical.Engineering.Faculty,
University of Belgrade, PO box 816, 11001 Belgrade,Yugoslavia

ABSTRACT:

The paper deals with the position and speed sensing in an environment of industrial servo drives equipped with resolver-type sensors. Problems of limited R/D converter resolution are outlined along with their influence on overall drive performance. Novice method for on-line R/D resolution change is proposed, and its software and hardware aspects are thoroughly examined. Primarily software based, proposed approach adapts the R/D resolution according to current shaft speed, so as to reduce the noise in feedback signals and optimize the drive performance. Experimentally verified, the method is proposed to potential users in the form of clear design guidelines.

1. INTRODUCTION:

Advanced servo drives with synchronous and induction motors demand high precision shaft sensors for the speed and the position measurement. Harsh industrial environment might include elevated temperatures, dust, oil vapors, noise and vibration that prevent the use of common optical transducers. When highly reliable operation in a severe environment is required, the shaft sensor commonly used is the robust electromagnetic resolver.

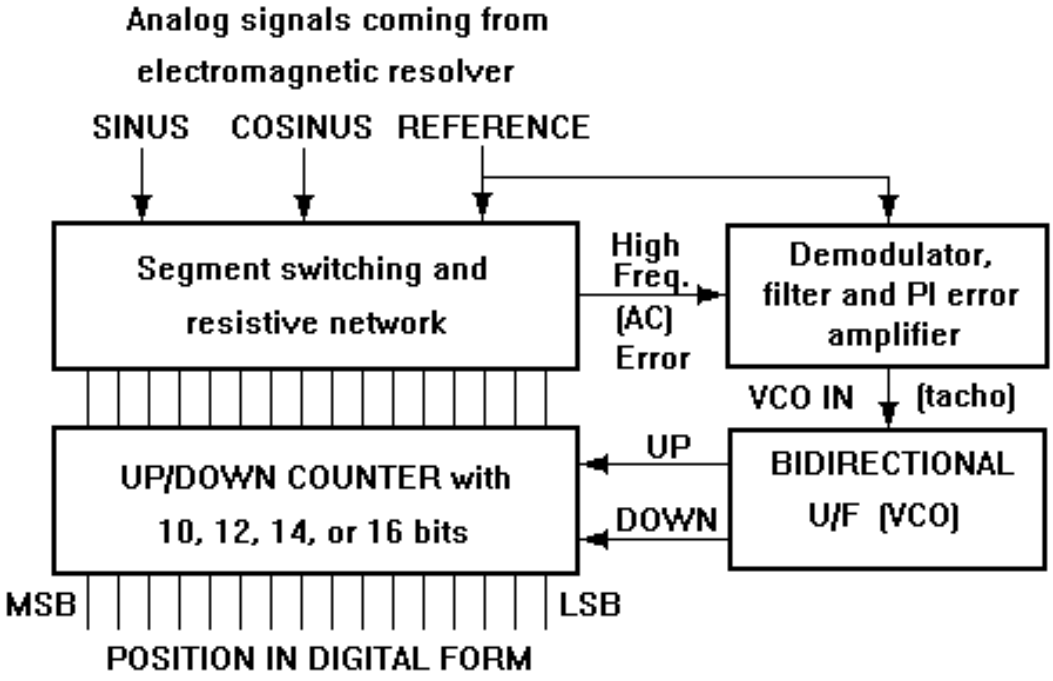
Resolver *sine* and *cosine* signals contain the information on the shaft position in an analog form. Ratiometric resolver to digital (R/D) converters are used for transforming the shaft position data in digital form, suitable for further processing. The resolution of conversion process might be preset from 10 to 16-bit with most of available R/D chips available on the market. High resolution gives the best precision of the position measurement and the lowest speed feedback ripple. Though, due to the finite topmost frequency of the VCOs and counters comprised within a R/D IC, the maximum shaft speed practicable in high resolution mode is limited. Hence, as the top speed of the drive increases, a lower R/D resolution must be preset, resulting in lower overall drive performance.

The drive performance might be significantly increased with variable resolution scheme, allowing the R/D converter's resolution to be adapted to the current shaft speed. In this paper, the method and application of novice, software implemented R/D resolution switching is proposed.

Basic analytical consideration and design guidelines are accompanied with experimental results, illustrating clearly visible improvement of overall drive performance.

2. R/D CONVERTER OPERATION WITH FIXED RESOLUTION:

Resolver-to-digital converters obtain the digital word related to the shaft position from analog signals coming from the *SINE* and *COSINE* detection windings of the resolver. Conversion process is ratiometric [1], and involves closed loop position tracking. Assumed position is present in an UP/DOWN counter (Fig.1) in the form of a digital word with 10, 12 14 or 16 bits. Resolver is normally excited by a low power, high frequency signal [2], having the frequency at least an order of magnitude higher than required bandwidth of the R/D tracking loop. Resistive network in Fig. 1 switches in and out internal resistors according to the status of corresponding counter bits. At its analog input, resistive net is connected to the *sine* and the *cosine* signals, obtained from the resolver detection windings. The net is arranged in such a way that an AC-error signal appears at the output. The error signal is proportional to the difference between the actual shaft position and the estimation contained as a word within the counter.



Фиг. 1: Басиц оператион оф тхе Р/Д цонвертер њитх фиџед ресолутион

High (excitation) frequency AC error is filtered demodulated, and processed through a PI (proportional - integral gain) block. Amplified error is used as the driving signal for a Bi-directional Voltage Controlled Oscillator; the BVCO generates the pulses at the “UP” output for positive values of VCO_IN signal (see Fig. 1); or, alternatively at the “DOWN” output in the cases whence the VCO_IN has a negative value. In both cases, the pulse frequency varies with the absolute value of the input signal. The BVCO is mostly [1] implemented as current controlled device.

The tracking loop is closed by feeding the BVCO output signals to the counter, providing for corrective action that forces the digital position estimate to track the actual shaft position. “UP” and “DOWN” pulses from the BVCO will increment or decrement the counter attempting to zero the error. The frequency of BVCO output is proportional to the rate of change of the shaft position, and hence, proportional to the shaft speed. The same way, the input to BVCO may be used as an analog representation of the shaft speed; the “tacho” signal.

Most of resolver-to-digital converters available [1] comprise a BVCO with the maximum pulse frequency below f_{max} = 1 MHz. Hence, the R/D converter will not be able to track the shaft position at a speed higher than ω_{max}[rps] = f_{max} [Hz] / 2^N; where N stands for the counter length in bits, and the ω_{max} designates the top speed in revolutions per second, assuming that resolver has one pair of poles. Generally, the top mechanical speed is obtained by dividing the value ω_{max} by the number of resolver pole pairs. The counter lenght N determines the resolution of the R/D converter, and might assume values of 10, 12, 14 or 16.

The best precision of the position measurement is obtained having N=16. In this case, full counter lenght is used (from b15=MSB to b0=LSB), the BVCO pulses affect the bits starting with b0, and the top speed ω_{max} is very small (example: with N=16, f_{max} = 1 Mhz and a 6-pole resolver, n_{max} = 305 [rpm]). In order to achieve higher speed, the R/D resolution has to be decreased to 14, 12 or 10, depending on the application requirements. For N=10, the resolution is at the minimum and the top shaft speed is n_{max}= 19531 [rpm] for 6-pole resolvers, and 58593 [rpm] for 2-pole devices. The BVCO clocking pulses do not affect six least significant bits within the 16-bit counter (b5-b0). The effect of one pulse is addition/subtraction of one (1) to/from a 10-bit digital word consisting of the bits b15..b6.

Accuracy and response speed of the tracking loop depends upon the excitation frequency, resistive net accuracy, the PI error gains and the counter lenght (10 - 16 bits). Generally, tracking loop bandwidth of the order of one tenth the excitation frequency may easily be achieved. The counter length N is preset by the user; two dedicated pins of the R/D chip has to be connected to logical 0 or pulled up to logical 1. Four possible combination will set N to 10,12, 14 or 16. Along the drive operation, the resolution remains fixed.

The resolution of position measurement is directly determined by the counter length. Hence, it varies from $2^{-10} * 2\pi$ to $2^{-16} * 2\pi$. The speed signal is most frequently obtained from the position information by means of a speed observer. Due to the fact that the speed observers intrinsically bring in the differentiation and filtering of the position signal, the speed feedback noise will increase as the R/D resolution decreases. Consequently, lower R/D resolution will limit the speed loop bandwidth, since the gains of the loop must be reduced due to the noise contained in the feedback signal.

Plenty of servo drive applications require both high precision at a low speed and the possibility to reach very high speed with lower precision. Machine tools application frequently calls for a high speed, rough cutting mode; followed by final low speed, high precision cutting. Spindle drives with automatic tool exchange call for extremely high top speeds at which the precision is not essential, but need as well high precision position measurement in the tool exchange mode. If the resolver with the R/D converter is used as the shaft sensor, the overall drive performances will be bonded by the necessity to choose and keep fixed one resolution of the R/D converter. When the top drive speed is high, so has to be the value of ω_{max} , and the user must select a low R/D resolution. Consequently, low speed performances will worsen; the speed loop bandwidth, suppression of the torque disturbances and the precision of the positioning will be inferior with respect to the case of a higher N; that would have been applied if the high speed requirement were not imposed.

The method and the means for a software based on-line resolution adaptation are analyzed and proposed in this paper, with the aim to achieve better utilization of the resolver and the R/D converter; and allow simultaneously high precision low speed operation as well as high operational speeds with decreased accuracy of the position measurement. The method with both hardware and software aspects of proposed on-line resolution switching has been thoroughly tested and build into the digital multiaxes servoamplifier [3], showing excellent results field test results.

3. ON-LINE RESOLUTION SWITCHING: HARDWARE ASPECTS

Drawbacks of the fixed resolution operation of R/D converter might be eliminated by selecting the resolution N lower at high shaft speeds, while switching to 14- or 16-bit resolution in low-speed high-precision mode of operation. The pins of the R/D (named SC1 and SC2 in the case of 2S82 part [1]) provided for hardware selection of R/D resolution might be software controlled, in which case their status, and hence, the R/D resolution might be changed on-line, during the drive operation.

On-line change of the R/D resolution basically means the change of the counter length; that is, a 10 => 12 resolution switching changes the counter format from [b15 ... b6] - 10 bit word, to 12 bit [b15...b4] word. Due to the fact that the shaft speed does not change significantly during the switching interval, and taking into account that the BVCO frequency is given f_{BVCO} [Hz] = 2^N ω[rps], the 10 => 12 resolution change must be followed by an increase of f_{BVCO} by four. The same way, reciprocal 12 => 10 resolution switching must be followed by a drop in the BVCO frequency by four.

The output frequency of the BVCO is controlled by the voltage level at the oscillators input (VCO IN signal in Fig. 1). This signal, in turn, is the output of an analog PI regulator, having the tracking error at the input. The VCO IN signal cannot change instantly, due to an inherently limited slope and response time of the PI block. Hence, inability to augment and diminish the VCO IN four times at the instant of the resolution switching will make impossible sudden changes in BVCO frequency. Therefore, a large tracking error will occur at the instant of SC1:SC2 switching, followed by the transient response of the tracking loop. In an environment of a servo drive with the speed loop, transient phenomena caused by the resolution change will provoke large torque spikes, speed errors, and the position error that is not acceptable. Severity of the problem might be observed better if the magnitude of the R/D internal speed error is considered: at each resolution change, the internal speed error is initially 400% - 100% = 300%.

It might be concluded from the above discussion that a means of step-changing the BVCO frequency by 4 must be found in order to obtain error-free, smooth resolution switching process; avoiding in such a way the interference with the speed and position loops. Solution to the problem is proposed hereafter, and applied on a 2S82 [1] R/D converter. Hardware details are given in Fig. 2.

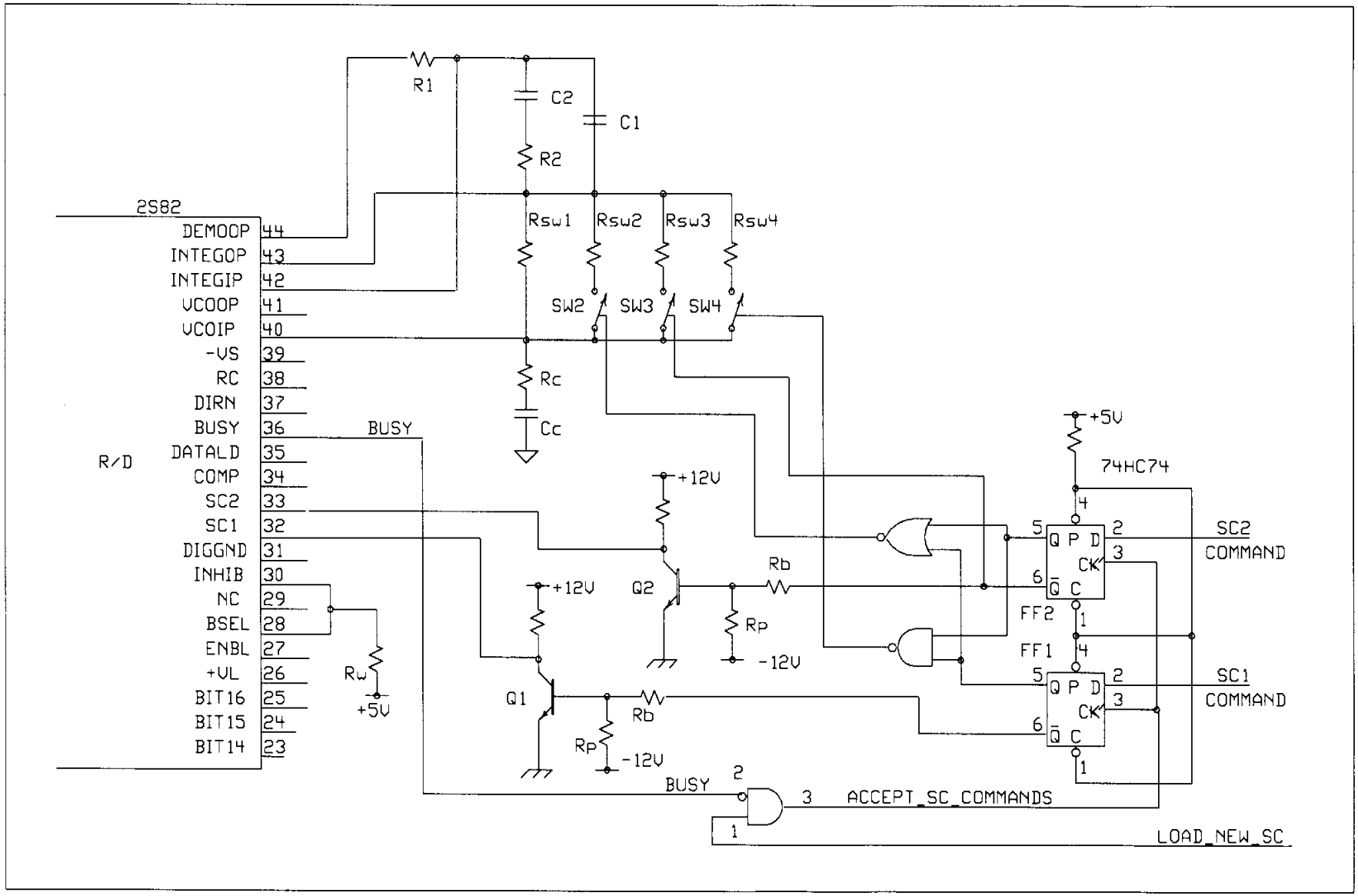

2S82
DEMOOP 44
INTEGOP 43
INTEGIP 42
VCOOP 41
VCOIP 40
-VS 39
RC 38
DIRN 37
BUSY 36
DATALD 35
COMP 34
SC2 33
SC1 32
DIGGND 31
INHIB 30
NC 29
BSEL 28
ENBL 27
+VL 26
BIT16 25
BIT15 24
BIT14 23
R/D
R1
C2
C1
R2
Rsw1
Rsw2
Rsw3
Rsw4
SW2
SW3
SW4
Rc
Cc
BUSY
+12V
Q2
Rb
Rp
-12V
Rw
+5V
Q1
+5V
74HC74
FF2
FF1
SC2
COMMAND
SC1
COMMAND
BUSY
ACCEPT_SC_COMMANDS
LOAD_NEW_SC

Figure 2. On-line R/D resolution switching: Hardware modification.

The output of the PI block in Fig. 1 (the VCO IN signal) is labeled as the INTEGOP pin of 2S82 in Fig. 2. The BVCO within the 2S82 R/D converter is a current controlled device; that is, the frequency of the clock pulses varies with the current supplied into the VCOIP input pin. Under assumption that the INTEGOP output is at a constant value, the BVCO pulse frequency is determined by the resistance connected between the INTEGOP and the VCOIP pin. Step change in the BVCO frequency might be obtained by changing this resistance four times at the instants of the resolution change. For this purpose, resistors R_{sw1}, R_{sw2}, R_{sw3}, and R_{sw4} are introduced in Fig. 2, along with associated analog switches SW2, SW3, and SW4.

Analog switches SW2, SW3, and SW4 should be set ON and OFF in function of the current resolution of the R/D converter. To avoid transient response of the tracking loop and reduce the risk of a large tracking error, equivalent resistance should always change by the factor of 4. For 10-bit resolution, all the analog switches should be OFF, and the value of equivalent resistance between INTEGOP and VCOIP pins is $R_e = R_{sw1}$. Passing to 12-bit resolution, the switch SW2 must close at the same instant when the code signals SC1 and SC2 change to 12-bit status. Since R_e in this state must be exactly 1/4 of the previous R_{sw1}, the value of R_{sw2} might be found as $R_{sw2} = 1/3\ R_{sw1}$. In such a way, equivalent resistance for the 12-bit resolution will be $1/4\ R_{sw1}$. Increasing further the resolution and passing from 12-bit to 14-bit resolution, the switch SW2 remains closed, while SW3 closes in exactly at the instant of the commutation on SC1-SC2 pins. In order to get $R_e = 1/16\ R_{sw1}$, the value of R_{sw3} must be exactly $1/12\ R_{sw1}$. Going further to 16-bit, the analog switch SW4 must be turned on, and both SC1 and SC2 control signals must be driven to the logic 1 level at the same time. Since the equivalent resolution in such case must be $1/64\ R_{sw1}$, the value of R_{sw4} is calculated as $1/48\ R_{sw1}$.

The resolution change basically modifies the format of the UP/DOWN counter. Hence, the effect of one BVCO pulse expressed in terms of estimated position in [rad] changes from $2\pi / 2^{10}$ for 10-bit resolution to $2\pi / 2^{16}$ that we have for 16-bit resolution. Potentially, this might change the closed loop gain of the R/D tracking loop 64 times, and significantly affect the position measurement accuracy and dynamics. The tracking loop gain variation is avoided by inserting $R_{sw1}..R_{sw4}$ and commutating the analog switches in the prescribed way. Along with the resolution change imposed by SC1-SC2 signals, the value of equivalent resistance between the INTEGOP and VCOIP pins is changed four times; causing the same INTEGOP level to provoke four times higher/lower BVCO frequency. In such a way, considering the signal flow from the INTEGOP pin to the counter, whatever the resolution the same level at the INTEGOP pin will produce always the same rate of change of the estimated position expressed in [rad/s]. Example: one BVCO pulse affects the estimated position 4 times less at 12-bit resolution that the same pulse when the resolution is 10-bit; but the INTEGOP - VCOIP equivalent resistance is 4 times smaller at 12 bit resolution, and the same INTEGOP voltage level makes BVCO count 4 times faster. As the consequence, the bandwidth and dynamics of the tracking loop does not change with the R/D resolution, the loop performs always in the same way.

At hardware design stage, care must be taken to the internal timing of the R/D device. Namely, after each BVCO clocking pulse, the data contained in the counter change, and the transition state may last 300-400 ns. During this interval, the counter outputs invalid data that should not be used. For this reason and due to internal R/D timing problems, the resolution must not be changed during the transition interval. Rather than that, the command for the resolution switching should be issued during the time interval when the counter data is stable. Even at the top (1MHz) BVCO frequency, there are 600-700 ns left to perform the resolution change.

The R/D converter marks the transition intervals by establishing high level at the BUSY pin (Fig. 2). In order to ensure that the R/D resolution changes are performed at the beginning of a "data stable" interval, flip-flops FF1 and FF2 are used. At their D inputs, the digital microcontroller outputs the code for SC1 and SC2 lines. The new status of SC1 and SC2 will determine the R/D resolution, as soon as FF1 and FF2 latch the data. For that to happen, the digital microcontroller must confirm the request by setting high the LOAD_NEW_SC line. Now, next falling edge of BUSY signal will provoke a rising edge at the FF's clock input, and new values for SC1 and SC2 will appear at Q outputs. These outputs will consequently set the status of SC1 and SC2 pins of the R/D, and determine the state of SW2, SW3, and SW4 analog switches. In the prescribed way, the resolution change will begin when the transition period ends, and adverse effects of switching during the transition will be avoided.

With the hardware prerequisites outlined above, the R/D tracking loop will suffer no error due to on-line resolution change, providing that components used in Fig. 2 are ideal ones. Some parasitic effects though, might provoke a small tracking error to occur at the switching instant, and these are listed in section 5. The next section deals with the software aspects of the resolution switching, and explains when and how the SC1, SC2 and LOAD_NEW_SC commands should be issued.

4. SOFTWARE IMPLEMENTATION

The basic requirements with respect to the counter length N (that is, the resolution in terms of the number of bits) are to use the maximum possible resolution, while taking care not to exceed the BVCO maximum frequency. Basic rules might be inferred from the relation that connects the shaft speed and the BVCO frequency: ω_{max}[rps] = f_{max} [Hz] / 2^N . When the shaft speed is in a decline, the BVOC frequency will reduce as well. For values $f_{BVCO} < 0.25\ f_{max}$, the resolution might be increased. Setting the next higher resolution in such a situation, the BVCO frequency will increase by a factor of 4. Since the previous value was $f_{BVCO} < 0.25\ f_{max}$, the change will not pass over the BVCO top frequency, and the integrity of the position measuring system will be preserved.

During the acceleration phase of the drive, the shaft speed will increase along with the BVCO pulse frequency. When coming close to the top BVCO frequency, the R/D resolution must be decreased to the next lower value, in order to allow for further shaft speed rise. The resolution drop will divide the f_{BVCO} by 4, making continued acceleration possible.

Decision on when and how to change the R/D resolution is made by the digital controller. Thresholds might be determined in terms of the shaft speed, or alternatively judged from the BVCO frequency. If the shaft speed were to determine the switching, a set of 6 thresholds would be necessary. For 12- and 14- bits both the upper and the lower limit would be necessary, while the minimum 10-bit and the maximum 16-bit resolutions will need only one threshold: lower (10-bit) and upper (16-bit).

Deriving the switching instants from the frequency of the BVCO pulses is natural choice, and much simpler to implement. It is sufficient to count the BVCO pulses, measuring in such a way the frequency. Only two limits have to be established: the minimum frequency (below which the resolution will be increased) and the maximum frequency (above which the resolution should be decreased).

The action of the digital controller consist in keeping the LOAD_NEW_SC signal in a passive state until the moment when the resolution change is required. At the instant of change, the lines SC1_COMMAND and SC2_COMMAND must be set first. Following that action, the LOAD signal should go into its active state, and remain active until at least on BUSY period passes; making sure in such a way that the flip flips latch the data.

5. PARASITIC PHENOMENA AND REMEDIES

Previous discussion assumed a linear relation between the BVCO input current and its output frequency. This linearity is essential for the proper operation of the proposed method. Namely, since each resolution change calls for a BVCO frequency change by a factor of 4, we designed the hardware in such a way that the change of the BVCO input current is ensured to be correct (that is, the BVCO input current will also change by a factor of 4). Now, if the BVCO input/output characteristics is linear, its output frequency will perform accordingly. Any error in the BVCO linearity will cause the pulse frequency to change at the instant of resolution switching by a factor higher or lower that 4. As a consequence, as explained above, the switching cause the tracking error and the transient response of the tracking loop. In order to avoid this problem, the switching thresholds (in terms of the BVCO pulse frequency) should be chosen in such a way that the corresponding points on the BVCO_IN / BVCO_OUT characteristics have the same ratio between the BVCO input current and the corresponding BVCO output frequency.

Special care should be taken in selecting the bipolar transistors Q1 and Q2 in Fig. 2, used for level-shifting the TTL signals up to the 12 V logic level; as well as their polarization resistors R_p, and R_b. Namely, the turn-on delay must be longer or equal to their turn-off delay; and that might be obtained by choosing the pull-up resistors, R_b and R_p. Having the turn-on delay longer, any transition on SC1 and SC2 pins of the R/D such as 10 => 01 will pass through the 11 state. Notice that the same transition will pass through the 00 state, providing that the turn-on is faster than turn-off. Due to the internal logic of the 2S82 R/D converter, it is essential to avoid passing through the 00 state. More specifically, 10 => 01 and 01 => 10 transitions correspond to the resolution change from 12 to 14 and vice versa. If transition passes shortly through the 00 state (that corresponds to the 10-bit resolution), the R/D converter will reset those counter bits that are not being used by the 10-bit resolution configuration. There are two bits that are being used by the 12- and 14-bit resolution, and not being used by 10-bit resolution. Hence, a short 00 interval will reset these bits and damage the data in the counter. In turn, the tracking loop will exhibit a transient response, attempting to correct the error. Having $\tau_{TURN\text{-}ON} < \tau_{TURN\_OFF}$ will completely eliminate the risk of generating the tracking error.

6. CONCLUSION

The paper proposes a software-based, simple to implement method of increasing the resolution of position feedback signal in an environment of the servo drive with electromagnetic resolver and the resolver-to-digital converter. The method requires minor hardware modifications that do not involve expensive parts and do not increase the hardware cost. Experimental verification shows and increase of the speed loop performance parameters by roughly 25%. The method is build into the series-produced DBM03 line of digital multiaxes servoamplifiers where it showed an excellent performance.

7. LITERATURE

[1] Analog Devices Inc., “Design-in reference manual: Data converters, amplifiers, special linear products, support components”, 1994.

[2] Hanselman, D.C.: “Resolver signal requirements for high accuracy resolver-to-digital conversion”, IEEE Transactions on Industrial Electronics, IE-37, 1990, pp 556-561

[3] Vickers Polymotor: “DBM03 installation guide and users manual”, 1994.