Reduction of Parasitic Spectral Components of Digital Space Vector Modulation by Real-Time Numerical Methods

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Abstract **- This paper presents the analysis of the voltage error caused by a finite resolution of the modulator. The suitable algorithm is proposed in order to eliminate offsets and to reduce parasitic components for as much as 15 dB. Essentially, the algorithm represents the numerical procedure of rounding the high-resolution amplitude products into lower resolution digital words that are to be loaded into the PWM counters. For a given resolution of the modulator, the suggested procedure considers the coupling between the phase residual errors and selects counter loads in such a way that the minimum voltage vector error is obtained. The presented analytical considerations are verified by experimental results. The spectra of the inverter output voltage, obtained in an experimental setup, illustrate the efficiency of the proposed algorithm in suppressing undesired spectral components of the inverter output.**

I. INTRODUCTION

Most industrial drives and UPS systems comprise a hard-switches three-phase inverter. By an appropriate modulation strategy, the inverter supplies the load with its VVVF output voltage corresponding to the voltage reference, or serves as an actuator in a closed-loop (CRPWM) control of the output current. The accuracy of digital modulator is proportional to the clock frequency of timers determining the width of the inverter firing pulses. The accuracy is inverse proportional to the PWM (commutation) frequency. Due to a finite accuracy of modulator, the inverter output voltage is usually contaminated by the parasitic DC component, subharmonics, and higher-order harmonics. Parasitic spectral components appear due to a finite resolution of setting the average output voltage within each PWM period, and may have adverse effects, such as the torque ripple in the case of AC drives, or the power transformer flux offset/saturation in the case of UPS systems.

Three phase inverters are commonly used as main tools in the field of AC drives, UPS systems, PWM line rectifiers, active power factor compensators, and many other applications involving three phase power conversion. Performances mostly required are that of the PWM power amplifier with minimized power losses, maximized input voltage utilization, and high output waveform (current, voltage) quality in the sense of a low THD, and "clear" spectrum, which means the absence of subharmonics. The state of art in the field of modulation techniques is the space vector modulation [2-6], outperforming other techniques in the DC bus utilization by 15% and offering reduced number of commutations within the switching period. The sequence of voltage vectors can be arranged in such a way that each transition involves the commutation of a single inverter leg [4]. This approach implies reversal of the sequences in successive switching periods;

thus, a symmetrical switching pattern is obtained [8] with centered phase voltage pulses and a harmonic benefit [1].

Whatever the chosen space vector sequencing is adopted, the time weighting of the output voltage vectors is defined by the voltage reference which is to be obtained. Whether the space vector or the regular sampled sinusoidal PWM, the modern implementation of modulator is always of digital type involving the microprocessor core and separate timer for each inverter leg. The digital modulator might be implemented through general purpose programmable timers as peripherals, or by using a microcontroller possessing a dedicated PWM hardware on board. For each switching period, the microprocessor calculates a multiple of the sine function and the voltage vector amplitude, and loads the three timers (or, alternatively, the registers of the dedicated PWM hardware) with appropriate values to obtain the desired pulse width of phase voltages. Assuming that the voltage reference does not change within the switching period, the width of phase voltage pulses determines the average output voltage value within the current switching period. The fundamental behavior of converter depends on these average values, but the commutation losses and current ripple are affected by the voltage vector sequence and usage of the redundant (111 and 000) voltage vectors. Any modulation strategy results in sinusoidal line-to-line voltages, while the phase voltages might contain triple harmonics [4], [8].

The resolution of the phase voltage setting is determined by the timer clock frequency and PWM frequency. For a typical microcontroller equipped with an internal hardware suitable for the PWM generation (HSO and WG unit of Intel MCS96), the resolution of timers is 250 ns. For the PWM frequency above 16 kHz, the resolution drops below the level of 8-bits. In such an application, significant voltage errors might occur due to rounding errors. Despite the trend of improving the performance of embedded microcontroller peripherals, the problem of the digital PWM modulator resolution will remain actual, since an increase of modulator's time resolution goes along with a requirement to elevate the PWM frequency of modern power converters.

The variable output frequency implies the asynchronous switching [2],[5]; that is, the PWM pattern is not a periodic function. In conjunction with cumulative errors in the output voltage caused by a finite resolution of the modulator, the asynchronous switching produces a continuous spectrum of the output voltage, rather than discrete one, as in the case of a strictly periodic PWM. In cases wherein the resolution of modulator lies below 8-bit, significant subharmonic components and even a parasitic DC level may be present in inverter output voltages.

The problem of voltage errors and parasitic harmonic components caused by a finite resolution of the digital modulator will adversely affect AC drive systems. Subharmonics may provoke an oscillating behavior of the induction motor. Moreover, low frequency components may cause torque ripples in both the induction and brushless AC drives, which, in turn, deteriorate the required performance and increase the risk of latent mechanical oscillations. In the case of UPS systems, the parasitic DC component will increase losses and eventually saturate the output power transformer, while low order harmonics may provoke the resonance of output filter.

Voltage supplied AC drives with closed digital current control loop are less sensitive to voltage errors originated by the rounding of load values of PWM timers. Still, parasitic frequency components may interfere with the complex poles of the current loop transfer function, and provoke purely damped or even sustained oscillations. This problem

may severely restrict the current loop gains applicable to the system and thus limit the resulting drive performance.

Rounding errors have more visible effects as the PWM frequency increases. For the purpose of reducing acoustic noise, size of power capacitors and chokes, and for an elevated response speed, the trend in the converter-fed AC drives and UPS systems longs to the use of PWM frequencies elevated up to ultra-sound frequencies. In order to obtain an acceptable current ripple, applications of AC drives involving motors with a very low leakage inductance (such as high frequency spindle motors) call for a very high PWM frequency as well. Hence, wherever a high quality of the output voltage waveform is required, the attention is to be paid to rounding errors; some means of rounding error compensation is essential for the clean output spectrum, and should be used along with the dead-time compensation and suppression of the input voltage ripple [9].

In this paper, the numerical algorithm is proposed in order to eliminate the offset and to reduce significantly parasitic spectral components, in the three-phase inverter output voltage, caused by a finite resolution of the modulator. Key features of the proposed algorithm are: the rounding error tracking, compensation of the past rounding error in each successive switching period, and implementation of specific rounding rules that guarantee minimum output error (voltage vector error). The rounding rules are developed considering minimization of the vector error in α–β plane and using the redundancy inherent to the three-phase inverter configuration; that is, the output voltage vector with only two coordinates is driven by the load-values of three timers within the digital modulator, i.e., by three inverter phase voltages.

The paper contains analytical considerations that prove validity of the proposed algorithm. Spectra obtained from an experimental setup illustrate suppression of parasitic spectral components obtained by the enhanced rounding and error tracking numerical routines for PWM pattern generation.

II. LINE-TO-LINE ERROR AND VOLTAGE VECTOR ERROR

The voltage reference and output voltage of the three-phase inverter may be interpreted in terms of their α–β components:

$$u_{\alpha} = u_a - \frac{u_b}{2} - \frac{u_c}{2}$$
$$u_{\beta} = \frac{\sqrt{3}}{2}(u_b - u_c). \qquad (1)$$

The inverter is capable of generating six discrete nonzero voltage vectors V1...V6 and the zero vector V0 (Fig.1). The zero vector can be generated as the switching state (000) or (111) [3-4]. The time-weighing of three vectors adjacent to the reference V0, V1, and V2 in Fig. 1 has to be accomplished in such a way that the output voltage average within the switching period *T* corresponds to the reference vector, which is assumed to be constant within the switching period.

In the following discussion, the time interval within the switching period *T,* when the output phase terminal A is switched to the (+) rail, is denoted as ON period or by $\tau_{on}(A)$, while the remainder of the switching period is denoted by $\tau_{off}(A) = T$ -

τ_{on}(A). The average phase voltage within the switching period, referred to the (-) rail, is $U_A = E\tau_{on}(A)/T$, where E is the DC-bus voltage.

Line-to-line voltages at the inverter output, as well as the output voltage vector in α–β representation, depend on the difference between phase voltages, that is, the difference between τ_{on}(A), τ_{on}(B), and τ_{on}(C). Hence, ON intervals may be offset by the same value, having no effect on the resultant output voltage vector. This degree of freedom gives possibility [8] to decrease the number of commutations within each switching period from 6 to 4. The possibility illustrates Fig. 1 related to the reference vector inside the segment 1 of the hexagon. Subtracting τ_{on}(C) from all three ON intervals will not change the average output vector. At the same time, the phase C output terminal will remain switched to the (-) rail during the segment 1. Other sequencing strategies [10] for the current ripple and the commutation frequency reduction are possible; in all of them, the accuracy of the output voltage setting depends on the resolution of timers/counters within the digital modulator, since the output of each timer determines ON period for each inverter phase.

ON intervals are calculated from the reference vector amplitude and argument (spatial orientation), involving a calculation of the sine function and a multiplication with the amplitude. Formulae depend on the sequencing strategy or the applied modulation technique. The following is an example related to the segment 1 in Fig. 1:

$$\begin{aligned}
\tau_{on}(\mathrm{A}) &= [\sin(\pi/3 - \theta) + \sin(\theta)]\, T\left|U_{\mathrm{ref}}\right| / E \\
\tau_{on}(\mathrm{B}) &= \sin(\theta)\; T\left|U_{\mathrm{ref}}\right| / E \\
\tau_{on}(\mathrm{C}) &= 0.
\end{aligned} \tag{2}$$

The microcontroller computes the values of τ_{on}(A), τ_{on}(B), and τ_{on}(C) in each switching period. The resolution (wordlenght) of calculated values is significantly higher than the resolution of the timers. Hence, the values τA, τB, and τC, rounded to the level of 1 timer LSB (Least Significant Bit) has to be loaded into three timers. The timer outputs will control the switching of three inverter phases, and the average value of the inverter output within the switching period will correspond to the voltage reference with an accuracy determined by the timer resolution.

The timer clock frequency f_{clk} and the switching period $T = 1/f_{pwm}$ determine the accuracy (resolution) of setting the average value of the phase voltage:

$$M = E_{dc}\frac{f_{pwm}}{f_{clk}}. \tag{3}$$

Example. For the DC-bus voltage of E_{dc} = 500 V, timer clock f_{clk} = 1 MHz, and f_{pwm} = 10 kHz, the quantum (resolution) of the phase voltage setting is M = 5 V. Hence, the actual values of the phase voltage will differ from the calculated ones. The errors due to the finite resolution are

$$\begin{aligned}
x &= [\tau_{on}(\mathrm{A}) - \tau A]E_{dc}f_{pwm}, \\
y &= [\tau_{on}(\mathrm{B}) - \tau B]E_{dc}f_{pwm}, \\
z &= [\tau_{on}(\mathrm{C}) - \tau C]E_{dc}f_{pwm}.
\end{aligned} \tag{4}$$

It is of interest to establish the relation between the resolution M and the maximum error of the output voltage vector in α–β plane, and to develop the rounding rules that minimize the error.

In the following analysis, the numbers $\tau_{on}(A)$ and τA will be interpreted taking into account the 1 LSB of the timer, in the sense that the $\tau_{on}(A)$ will be considered as a real number having τA as the integer part, and $\tau_{on}(A) - \tau A$ as the decimal part. The decimal part will vary within an interval of 1 timer LSB, which will correspond to the phase voltage variation of M.

The amplitude of the error vector $\Delta U_{\alpha\beta}$ can be expressed in terms of x, y, and z by (see Equation 1):

$$\left|\Delta U_{ab}\right|^2 = (x - \frac{1}{2}y - \frac{1}{2}z)^2 + \frac{3}{4}(y - z)^2 = x^2 + y^2 + z^2 - xy - yz - zx \qquad (5)$$

where x, y, and z are given by relations (4).

Whether the rounding is performed to the first integer higher than the real value, first integer lower than the real value, or closest integer, the values x, y, and z will lie in the interval M. Let us assume $x \geq y \geq z$ and $x - z \leq M$. Then, introducing $y - z = m_1 \geq 0$ and $x - z = m_2 \geq m_1$, the error $\Delta U_{\alpha\beta}$ can be expressed by $|\Delta U_{\alpha\beta}|^2 = m_1^2 - m_1 m_2 + m_2^2$. Since the second partial derivatives of this expression are positive, the vector error has the minimum inside region $M \geq m_2 \geq m_1 \geq 0$. The maximum value of the error lies at the edge of the region. With $m_2 = M$ and m_1 either 0 or M we get $|\Delta U_{\alpha\beta}|^2_{max} = M^2$. At the same time, M stands for the maximum error of the line-to-line voltage at the inverter output.

An example where $x = M - \varepsilon$, $y = \varepsilon$, and $z = \varepsilon$ may illustrate the possibility to reduce voltage errors caused by the finite modulator resolution. If ε is an infinitesimal quantity, the vector error is $|\Delta U_{\alpha\beta}| = M$. If we increment the rounded value τA by 1 LSB of the timer, the residual part x will be reduced by M, and new values of phase voltage errors will be $x' = -\varepsilon$, $y' = \varepsilon$, and $z' = \varepsilon$. After the increment, the vector error becomes $|\Delta U_{\alpha\beta}| = 2\varepsilon$.

The vector error $|\Delta U_{\alpha\beta}|_{max} = M$ and line-to-line error $|x - y|_{max} = M$ obtained with the standard rounding procedure will be compared to the maximum errors of the enhanced rounding technique, described in the following section.

III. ANALYTICAL DERIVATION OF ROUNDING RULES THAT REDUCE VOLTAGE ERRORS

For the sake of brevity in developments, the vector error can be expressed in terms of the differences a, b, and c of the phase voltage errors x, y, and z from their mean value referred as to the gravity point g:

$$g = \frac{x + y + z}{3}$$

$$a = x - g, \quad b = y - g, \quad c = z - g$$

$$a + b + c = 0$$

$$\left|\Delta U_{ab}\right|^2 = x^2 + y^2 + z^2 - xy - xz - yz$$
$$= \frac{3}{2}(a^2 + b^2 + c^2). \qquad (6)$$

Considering $|a - b| = |x - y| \le M$ and $a + b + c = 0$, we conclude that absolute values of a, b, and c are bounded by $2M/3$. If $a > 2M/3$, $(-b - c)$ must be greater than $2M/3$ and consequently either b or c must be less than $-M/3$. In this case, $(a - b)$ or $(a - c)$ will exceed M. Hence,

$$|a| \le \frac{2}{3}M, \quad |b| \le \frac{2}{3}M, \quad |c| \le \frac{2}{3}M. \qquad (7)$$

Whatever the rounding rule is developed, the final result will consist in incrementing/decrementing one or more of rounded values τA, τB, and τC so to reduce the vector error and line-to line error. In the following, it will be shown that all of these "useful operations" can be reduced to two basic ones: (i) Incrementing the timer load τX for one phase; (ii) Decrementing the timer load τX for one phase. The proof will be deduced from a set of statements listed hereafter and labeled by P1..P7. For the sake of brevity, expressions (+|-|0, +|-|0, +|-|0) will stand for the post-rounding intervention (increment, decrement or no interventions on τA, τB, and τC). Post-intervention quantities are marked by a prime (x') and obvious proofs are omitted.

P1:

Incrementing or decrementing all the values by 1 LSB does not change the vector error. This is proved by the following considerations:

(+, +, +):	(-, - ,-):
$x' = x - M,\ y' = y - M,\ z' = z - M$	$x' = x + M,\ y' = y + M,\ z' = z + M$
$g' = g - M$	$g' = g + M$
$a' = x' - g = a,\ b' = b,\ c' = c$	$a' = x' - g' = a,\ b' = b,\ c' = c$
$\lvert\Delta U_{\alpha\beta}\rvert' = \lvert\Delta U_{\alpha\beta}\rvert$	$\lvert\Delta U_{\alpha\beta}\rvert' = \lvert\Delta U_{\alpha\beta}\rvert$

P2:

Modification of a rounded value by more than 1 LSB always increases the voltage error. Proof below is given for one out of 6 possible cases: τA incremented by 2 LSB, (++, 0, 0):

$$x' = x - 2M,\ y' = y,\ z' = z$$
$$g' = g - \frac{2}{3}M$$
$$a' = x' - g' = x - 2M - g + \frac{2}{3}M = a - \frac{4}{3}M$$
$$b' = b + \frac{2}{3}M,\ c' = c + \frac{2}{3}M$$
$$\left|\Delta U_{ab}\right|'^2 = \frac{3}{2}(a'^2 + b'^2 + c'^2)$$
$$= \frac{3}{2}(a^2 - \frac{8}{3}aM + \frac{16}{9}M^2 + b^2 + \frac{4}{3}bM + \frac{4}{9}M^2 + c^2 + \frac{4}{3}cM + \frac{4}{9}M^2)$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \left|\Delta U_{\mathrm{ab}}\right|^2 + \frac{3}{2}\left(\frac{8}{3}M^2 + \frac{12}{3}bM + \frac{12}{3}cM\right)$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \left|\Delta U_{\mathrm{ab}}\right|^2 + M(4M - 6a)$$

$$|a| \le \frac{2}{3}M \Rightarrow M(4M - 6a) \ge 0 \Rightarrow \left|\Delta U_{\mathrm{ab}}\right|' \ge \left|\Delta U_{\mathrm{ab}}\right|.$$

P3:

Simultaneous increment in one phase and decrement in the other increases the error. Case: τA incremented, τB decremented, (+, - ,0):

$x' = x - M, \quad y' = y + M, \quad z' = z$

$g' = g$

$a' = x' - g' = x - M - g = a - M$

$b' = y' - g' = y + M - g = b + M$

$c' = c$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \frac{3}{2}(a'^2 + b'^2 + c'^2)$$

$$= \frac{3}{2}(a^2 - 2aM + M^2 + b^2 + 2bM + M^2 + c^2)$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \left|\Delta U_{\mathrm{ab}}\right|^2 + 3M(M - a + b)$$

$$|a - b| \le M \Rightarrow 3M(M - a + b) \ge 0 \Rightarrow \left|\Delta U_{\mathrm{ab}}\right|' \ge \left|\Delta U_{\mathrm{ab}}\right|.$$

P4:

Simultaneous increments in all three phases (+, +, +) *has no effect on the error, since* $a' = a$, $b' = b$, *and* $c' = c$.

P5:

Simultaneous decrements in all three phases (-, -, -) *has no effect on the error, since* $a' = a$, $b' = b$, *and* $c' = c$.

P6:

The effect of simultaneous increments in two phases is equivalent to the decrement in the third one:

(+, +, 0) ⇔ (+, +, +) + (0, 0, -) ⇔ (0, 0, -)

P7:

The effect of simultaneous decrements in two phases is equivalent to the increment in the third one:

(-, -, 0) ⇔ (-, -, -) + (0, 0, +) ⇔ (0, 0, +)

From P1..P7 we conclude that all the "useful" (yielding error reduction) post-rounding operations are equivalent to the two basic "useful operations": (i) The post-rounding increment of only one timer load value by 1 timer LSB. (ii) The post-rounding decrement of only one timer load value by 1 timer LSB. In order to establish an improved rounding algorithm, it is necessary to analyze effects of aforementioned operations.

Post-rounding increment. Case: τA incremented by 1 LSB, (+, 0, 0):

$$x' = x - M, \quad y' = y, \quad z' = z$$

$$g' = g - \frac{1}{3} M$$

$$a' = x' - g' = x - M - g + \frac{1}{3} M = a - \frac{2}{3} M$$

$$b' = b + \frac{1}{3} M$$

$$c' = c + \frac{1}{3} M$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \frac{3}{2}(a'^2 + b'^2 + c'^2)$$

$$= \frac{3}{2}(a^2 + b^2 + c^2 + \frac{2}{3} M^2 - 2aM)$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \left|\Delta U_{\mathrm{ab}}\right|^2 + M^2 - 3aM. \tag{8}$$

Post-rounding decrement. Case: τA decremented by 1 LSB, (-, 0, 0):

$$x' = x + M, \quad y' = y, \quad z' = z$$

$$g' = g + \frac{1}{3} M$$

$$a' = x' - g' = x + M - g - \frac{1}{3} M = a + \frac{2}{3} M$$

$$b' = b - \frac{1}{3} M$$

$$c' = c - \frac{1}{3} M$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \frac{3}{2}(a'^2 + b'^2 + c'^2)$$

$$= \frac{3}{2}(a^2 + b^2 + c^2 - \frac{2}{3} M^2 + 2aM)$$

$$\left|\Delta U_{\mathrm{ab}}\right|'^2 = \left|\Delta U_{\mathrm{ab}}\right|^2 - M^2 + 3aM. \tag{9}$$

Thus, the vector error will be reduced by incrementing the timer load value by 1 LSB for one of the phases if the distance (*a*, *b*, or *c*) between the residual error of that phase (*x*, *y*, or *z*) and the gravity point *g* (mean value of all residues) is greater than *M*/3. The same holds for the action of decrementing and the distance (*a*, *b,* or *c*) lower than *M*/3. Consequently, the situation where none of |*a*|, |*b*|, and |*c*| is greater than *M*/3 calls for no intervention; that is, the vector error cannot be reduced after the standard rounding procedure. If one of the distances *a*, *b*, and *c* has the absolute value greater than *M*/3, then

the timer load value has to be incremented or decremented, depending on the sign of the respective distance. We also have to consider the possibility where two, or all three distances *a*, *b,* and *c* may have the absolute value greater than *M*/3. Notice, a situation where all three numbers |*a*|, |*b*|, and |*c*| are greater than *M*/3 is not possible, since the maximum distance between *a*, *b*, and *c* is *M.* Namely, since $a + b + c = 0$, there are two positive or two negative numbers, for $b < -M/3$, $c < -M/3$, and $a = -b - c > 2M/3$, which results in the contradiction $a - b > M$ and $a - c > M$.

A situation where there are two numbers among *a, b,* and *c* with absolute value greater than *M*/3 is possible but only if these numbers are with opposite signs (such as $a = 0.4M$, $b = -0.4M$, and $c = 0$; if these two numbers are of the same sign and having their absolute values greater than *M*/3, then the distance from the third number will be greater than *M*). In these cases, the suppression of the vector error will be more efficient if the operation is accomplished in the phase where the distance (*a, b, c*) of the residual error (*x, y, z*) from the gravity point *g* has larger absolute value than the other one (see Eqs. 8 and 9). Notice, it is already proved that subsequent operations in both phases, incrementing the first and decrementing the second one (see the proof of P3), increases the vector error under any circumstances.

It is of particular importance to note the following: *If the phase selected for the operation is the first one (for example, the phase with the distance a = x - g), then both distances b and c of remaining phases are with the same sign, opposite to the sign of the distance in the selected phase. Proof: Taking a > M/3, |a| > |b| and |a| > |c| assumption b > 0 leads to conclusion that c = - a - b has the absolute value |c| > |a| which is in contradiction with |a| > |c|.*

Hence, the algorithm minimizing the vector error for the given resolution of modulator may be carried out by the following steps:

#1 Perform the standard rounding procedure.

#2 Calculate the residual values *x*, *y* and *z* (real rounded values).

#3 Determine the gravity point *g* or the mean value of the residues *x, y,* and *z.*

#4 Calculate the distances *a, b,* and *c* of the residues from the gravity point *g.*

#5 Locate the phase with the maximum absolute distance.

#6 If the distance is positive and greater than *M*/3, increment the timer load value for the located phase.

#7 If the distance is negative and less than - *M*/3, decrement the timer load value for the located phase.

Fig. 2 illustrates the proposed procedure. The procedure cuts the vector error in each PWM period to the minimum, for the given resolution of digital modulator. Though reduced, residual errors in successive PWM cycles might accumulate in a parasitic DC and/or low frequency spectral component of the converter output voltage. In order to alleviate this problem, an error tracking/correcting scheme is nested (Fig. 2) within the enhanced rounding algorithm. Before entering the rounding/post-rounding routine, high resolution sine-amplitude products $\tau_{on}(a)$, $\tau_{on}(b)$, and $\tau_{on}(c)$ are added to respective past residues $\Delta\tau A$, $\Delta\tau B$, and $\Delta\tau C$ to obtain high resolution pulse widths $\tau_{on}(A)$, $\tau_{on}(B)$, and $\tau_{on}(C)$ that are entering the rounding block in Fig. 2. After the enhanced rounding block, residues $\Delta\tau A_{(n-1)}$, $\Delta\tau B_{(n-1)}$, and $\Delta\tau C_{(n-1)}$ for the next period of PWM are determined as

differences between high resolution pulse widths $\tau_{on}(A)$, $\tau_{on}(B)$, and $\tau_{on}(C)$ and timer loads $\tau'A$, $\tau'B$, and $\tau'C$.

In such a way, the sum of all passed errors is kept below the level of 1 timer LSB, which suppresses DC and low frequency parasitic components of the output spectrum.

IV. REDUCTION OF THE LINE-TO-LINE ERROR AND VECTOR ERROR BY THE PROPOSED TECHNIQUE

Let us assume that the intervention is performed in the first phase (A) and that $a = x - g > M/3$. The assumption does not affect the general character of the subsequent considerations. Distances *a, b,* and *c* before the intervention as: $a = p + M/3$ with $0 < p < M/3$ (regarding the condition for intervention $M/3 < a < 2M/3$); $b = -q$ with $0 < q < p + M/3$ (see the proof, if the first phase is selected for the intervention and $a > 0$, then $b < 0$, $c < 0$, $|b| < |a|$, and $|c| < |a|$); $c = -a - b = q - p - M/3$. After the intervention (increment in phase A by 1 LSB), the distances become

$$\begin{aligned} a' &= a - \frac{2}{3}M = p - \frac{1}{3}M \\ b' &= b + \frac{1}{3}M = \frac{1}{3}M - q \\ c' &= c + \frac{1}{3}M = q - p. \end{aligned} \tag{10}$$

Since all values of *a, b,* and *c* lie inside an interval of width *M*, and the intervention results in $a' = a - 2M/3$, $b' = b + M/3$, and $c' = c + M/3$, the distance a' will be the lowest among $a', b',$ and $c',$ i.e., $a' < b'$, and $a' < c'$. Thus, the greatest line-to-line error after the intervention will be either $y' - x' = b' - a'$ or $z' - x' = c' - a';$

$$c'-a' = \frac{1}{3}M + q - 2p > 0, \quad \text{or} \quad (c'-a')_{\max} = \frac{2}{3}M, \quad \text{for} \quad q = \frac{1}{3}M \quad \text{and} \quad p = 0$$

$$b'-a' = \frac{2}{3}M - q - p > 0, \quad \text{or} \quad (b'-a')_{\max} = \frac{2}{3}M, \quad \text{for} \quad p = 0 \quad \text{and} \quad q = 0.$$

Hence, the maximum line-to-line error obtained after the application of the proposed algorithm is $2M/3$.

It is of interest to determine the effect of the intervention on the vector error as well. Under the same assumptions as above, we arrive at

$$\begin{aligned} \left|\Delta U_{ab}\right|'^2 &= \frac{3}{2}(a'^2 + b'^2 + c'^2) \\ &= 3(p^2 + q^2 + \frac{1}{9} - \frac{p}{3} - \frac{q}{3} - pq) \\ &= f(p,q). \end{aligned} \tag{11}$$

The second partial derivatives of the function $f(p,q)$ within the region $[0 < p < M/3,\ 0 < q < (p + M/3)]$ are strictly positive and consequently the maximum of $f(p,q)$ does not exist inside the region. By the analysis of region borders, the maximum of $f(p,q)$ is found in two points: $(p = 0, q = 0)$ and $(p = 0, q = M/3)$. In both of these points,

(12)

$$\left|\Delta U_{\mathrm{ab}}\right|^{2}_{\max} = \frac{1}{3}M^{2}.$$

Now, maximum line-to-line errors and maximum vector errors before and after the implementation of the proposed algorithm can be summarized into the following table.

Table 1. *Maximum line-to-line errors and vector errors.*

Maximal errors	$\left\|\Delta U_{\mathrm{ab}}\right\|^{2}_{\max}$	$\left\|\Delta U_{\mathrm{ab}}\right\|_{\max}$	$\left\|\Delta U_{ab}\right\|_{\max}$
After the standard rounding	M^{2}	M	M
After the application of the proposed algorithm	$\frac{1}{3}M^{2}$	$\frac{1}{\sqrt{3}}M$	$\frac{2}{3}M$

V. EXPERIMENTAL VERIFICATION

To validate the analysis, the experimental setup was build comprising a 3-phase inverter prototype with MOSFET power switches, and an Intel 8096 microcontroller, performing the function of the digital pulse width modulator. Inverter prototype was supplied from 60V DC voltage source. The dead-time was set to 400 ns. The inverter load was a symmetrical RL 3-phase load with the time constant τ = L/R = 5 ms. The output voltage spectrum was obtained from line-to-line output voltages attenuated by means of resistive dividers and fed to the input of the spectrum analyzer.

The space vector modulation with centered pulses [8] is performed utilizing the HSO unit of the 8096 microcontroller. The time resolution of HSO unit was 2 μs, while the PWM period was set to 256 μs. An interrupt routine is invoked each 128 μs, programming alternatively the rising and falling edge of the phase voltages. Within each interrupt, a sine-amplitude multiplication is performed, followed by the enhanced rounding routine and the error tracking/correcting block.

In order to reduce the execution time, the enhanced rounding is performed by means of reading a look-up table from the EPROM, coded with decisions related to post-rounding incrementing/decrementing. At the execution time, a 12-bit table pointer is obtained from the three rounding residues *x*, *y*, and *z*. The residues are scaled to the level of 4-bit binary constants. The 12-bit pointer is determining the location in the look-up table containing optimal post-rounding intervention for the given residues. In such a way, the operations illustrated in the flow chart in Fig. 2 are not executed within an interrupt, but during the preparation of data for the look-up table, at the code compilation time. Fig. 2 does not illustrate an overflow prevention feature included in the interrupt routine. This feature consists in the following. (i) The intervention (-, 0, 0) is substituted with the intervention (0, +, +), if $\tau A = 0$ before the post-rounding intervention. (ii) The intervention (+, 0, 0) is substituted with (0, -, -) if $\tau A = \tau A_{max}$ (= 128, in the experimental setup) before the post-rounding intervention. The same holds for the phases B and C. According to P6 and P7, the aforementioned overflow prevention feature does not affect the vector error.

The suggested rounding techniques for space-vector PWM were implemented by the program coded in assembly language according to the flow chart in Fig. 2. The program comprises possibilities of excluding error tracking/correcting routine. For the purpose of comparison, the program also features the plain rounding PWM, used in experiments.

For the fundamental output frequency of 56 Hz and amplitude of the reference vector at the edge of the saturation (maximum output voltage), line-to-line voltage spectra are shown in Figs. 3-5. The frequency of 56 Hz has been chosen in order to avoid interference with the noise from the mains frequency and its multiples. Fig. 3 visualizes the spectrum for both the enhanced rounding and error tracking/correcting switched on. In Fig. 4, the line-to-line voltage spectrum is shown for the same output frequency and amplitude, but with the error tracking switched off. As the result, parasitic subharmonics close to 6 and 20 Hz appear, being 12 dB more emphasized with respect to the spectrum in Fig. 3. The spectrum obtained by using the plain (standard) rounding is shown in Fig. 5. Comparing spectra in Figs. 3 and 5 one can conclude that the application of the proposed real-time numerical methods suppresses parasitic spectral components for 10-15 dB, at the output frequency of 56 Hz.

Figs. 6 and 7 present the spectra of the line-to-line output voltage at the fundamental frequency of 18 Hz and $|U_{\text{ref}}| = 0.33\ U_{\text{max}}$. Figs. 6 and 7 correspond to the application of the proposed real-time numerical algorithm and plain rounding, respectively. In virtue of the figures, the proposed method reduces the spectral parasitics in all frequency ranges. Moreover, in the vicinity of 300 Hz, the reduction is as much as 20 dB.

Spectra in Figs. 3-7, were measured from sets of line-to-line voltage samples taken within the time span of 1.6 seconds. Due to the fact that the PWM pattern is not strictly a periodic function when the asynchronous switching is applied, measured spectra may depend upon the relative position of PWM pattern within the period of fundamental frequency. Therefore, for the purpose of more precise comparison, the spectral measurements were also accomplished by using the average feature of the spectrum analyzer. For total of 512 successive measurements, average spectra are given in Figs. 8 and 9, in the logarithmic scale. The sum of successive spectral data is rescaled internally by the spectrum analyzer, taking into account the number of measurement runs. Fig. 8 presents the spectral data for the output frequency of 56 Hz, maximum amplitude of the output voltage, and complete error reduction mechanism from Fig. 2. Fig. 9 shows the spectrum obtained by the plain rounding. Most emphasized parasitic components of the spectrum are marked in Figs. 8 and 9, and then arranged into Table 2.

Table 2. *Suppression of peak parasitic spectral components at 56Hz output.*

Fig. 8	Frequency [Hz]:	11.2	23.7	27.5	88.7	133	234	312	426
data:	Amplitude [dB]:	- 96	- 96	- 95	- 92	- 95	- 93	- 91	- 89
Fig. 9	Frequency [Hz]:	13.7	22.5	32.5	73.7	112	167	223	448
data:	Amplitude [dB]:	- 105	- 107	- 106	- 108	- 99	- 99	- 95	- 95
ΔA	Suppression of parasitics [dB]:	9	11	11	16	4	6	4	6

Table 2 visualizes the efficiency of the proposed algorithm in suppressing parasitic components. Moreover, the DC component is reduced for approximately 15 dB (see also Figs. 8 and 9).

VI. CONCLUSION

The suitable real-time numerical algorithm was proposed in order to eliminate the offset (DC component) and to suppress as much as possible undesired spectral components in the output voltage of the three-phase inverter. Recall, the parasitic DC component, subharmonics, and higher-order harmonics appear due to a finite resolution of the modulator. Therefore, the suggested algorithm includes special way of tracking of the rounding error and novel method of compensation of the post rounding error in each subsequent switching period. Taking into account the redundancy inherent to the three-phase inverter configuration, the post-rounding rules were developed so as to minimize the vector error in the α–β plane.

The developed algorithm was implemented in real-time by the ASSEMBLER program on an experimental setup built by using the microcontroller INTEL 8096. The set of experimental measurements has been done with several programs that include different way of rounding with or without the suggested error tracking. The spectra obtained by using the complete algorithm, proposed in the paper, demonstrate the efficiency of algorithm in both the removing of the offset and in the suppressing of parasitic spectral components that contaminate the output voltage of the three-phase inverter.

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FIGURE CAPTIONS

Fig. 1. *Active and zero vectors at the three-phase inverter output and the related symmetrical PWM pattern.*

Fig.2. *Block diagram of the proposed real-time numerical algorithm.*

Fig. 3. *The spectrum of line-to-line output voltage measured at the output frequency of 56 Hz. Both the proposed rounding procedure and error tracking are applied.*

Fig. 4. *The spectrum of line-to-line output voltage measured at the output frequency of 56 Hz. The proposed rounding procedure is applied without the error tracking.*

Fig. 5. *The spectrum of line-to-line output voltage measured at the output frequency of 56*

Hz. The plain rounding is applied; the proposed rounding procedure and error tracking are ommited.

Fig. 6. *The spectrum of line-to-line output voltage measured at the output frequency of 18 Hz. Both the proposed rounding procedure and error tracking are applied.*

Fig. 7. *The spectrum of line-to-line output voltage measured at the output frequency of 18 Hz. The plain rounding is applied; the proposed rounding procedure and error tracking are ommited.*

Fig. 8. *The average spectrum of line-to-line output voltage measured at the output frequency of 56 Hz. Both the proposed rounding procedure and error tracking are applied.*

Fig. 9. *The average spectrum of line-to-line output voltage measured at the output frequency of 56 Hz. The plain rounding is applied; the proposed rounding procedure and error tracking are ommited.*

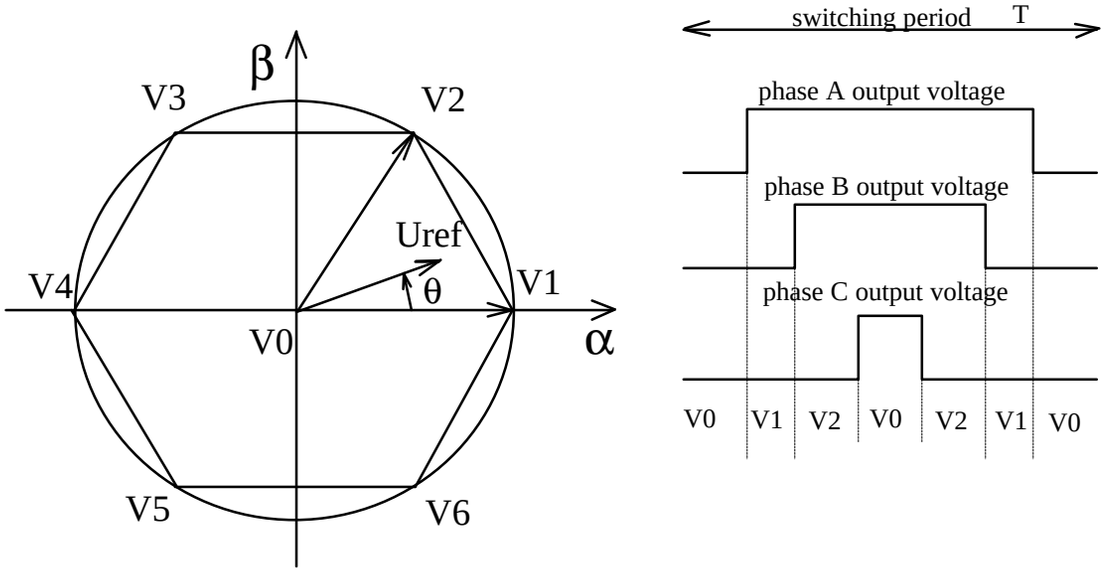
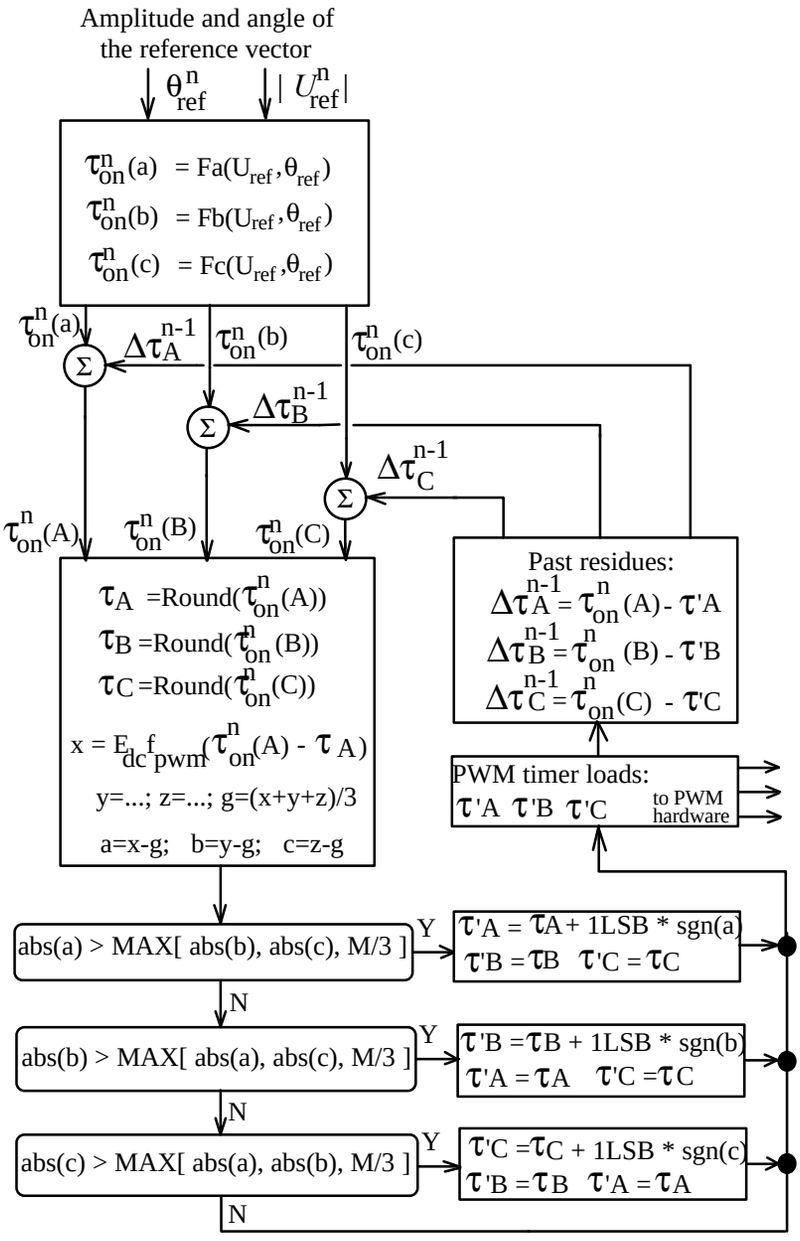


Fig. 1


Amplitude and angle of the reference vector
θ^n_ref
| U^n_ref |
τ^n_on(a) = Fa(U_ref, θ_ref)
τ^n_on(b) = Fb(U_ref, θ_ref)
τ^n_on(c) = Fc(U_ref, θ_ref)
Σ
Δτ^n-1_A
Δτ^n-1_B
Δτ^n-1_C
τ^n_on(A)
τ^n_on(B)
τ^n_on(C)
τ_A =Round(τ^n_on(A))
τ_B =Round(τ^n_on(B))
τ_C =Round(τ^n_on(C))
x = E_dc f_pwm(τ^n_on(A) - τ_A)
y=...; z=...; g=(x+y+z)/3
a=x-g; b=y-g; c=z-g
Past residues:
Δτ^n-1_A = τ^n_on(A) - τ'A
Δτ^n-1_B = τ^n_on(B) - τ'B
Δτ^n-1_C = τ^n_on(C) - τ'C
PWM timer loads:
τ'A τ'B τ'C
to PWM hardware
abs(a) > MAX[abs(b), abs(c), M/3]
Y
τ'A = τA + 1LSB * sgn(a)
τ'B = τB τ'C = τC
N
abs(b) > MAX[abs(a), abs(c), M/3]
Y
τ'B = τB + 1LSB * sgn(b)
τ'A = τA τ'C = τC
N
abs(c) > MAX[abs(a), abs(b), M/3]
Y
τ'C = τC + 1LSB * sgn(c)
τ'B = τB τ'A = τA
N